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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2827	#6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,151	BOYLAN ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,13 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,13 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The present Office Action is responsive to Applicant's amended Response filed December 16, 2002 as Paper No. 5. The Examiner acknowledges the amendments to Claims 1-3, 7, 13 and 14, and the cancellation of Claims 11 and 12. Claims 1-10, 13 and 14 remain pending in the instant amended Application.

Claim Objections

2. Claims 13 and 14 are objected to because of the following informalities:

In Claim 13, line 2: "comprise" should be changed to --comprises--.

In Claim 14, line 2: "comprise" should be changed to --comprises--.

Appropriate correction is required.

Rejections Based On Prior Art

3. The following references were relied upon for the rejections hereinbelow:

Iversen et al. (US 6,384,492 B1)	Patel et al. (US 6,366,467 B1)
McDonnal (US 5,075,821)	Li (US 6,525,944 B1)

Claim Rejections - 35 USC § 102/103

4. Claims 1-10, 13 and 14 are rejected under 35 U.S.C. 102(e) as anticipated by Patel et al. or, in the alternative, under 35 U.S.C. 103(a) as obvious over Patel et al. in view of Li.

Rejection #1 of Claim 1:

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-7, 9, 10 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Patel et al.

As to Claim 1, Patel et al. discloses, in Fig. 5, an adapter (interposer) 506 comprising: a first (top) and a second (bottom) surface; first interconnects, i.e., the pads, not shown, on the first surface of adapter 506 that receive and electrically connect the BGA bumps of carrier 502 to adapter 506; second interconnects (pins 508; col.4: 62-66) on the second surface; since second interconnects 508 supply power to step down converter (SDC) 518 on carrier 502 (col.4: 66), then at least one connective path inherently exists between the first and second interconnects; a signal modifying circuit (comprising input capacitor 522 and input inductor 524) between the first interconnects and second interconnects 508, as disclosed in an alternate case of the Fig. 5 embodiment wherein said input capacitor 522 and input inductor 524 are mounted on the adapter 506, as in the embodiment of Fig. 3 (Fig. 3 and col.3: 63-64; Fig. 5 and col.5: 14-15); the second interconnects 508 are *pins* that are **used** as *socket connects* in Patel et al. (col.4: 62-66). However, since the Applicant **does not positively claim a**

structure such as a printed circuit board having through holes (or, for that matter, a surface mounted socket structure) for receiving the pins, then the Applicant's recitation of "through hole connect" is nothing more than the recitation of a pin with an **intended use** (i.e., a pin *for connection to some unclaimed structure having a through hole*). Accordingly, the Examiner reads the limitation "through hole connect" as a pin which is met by any of the pins 508 of Patel et al. which may be used as a *socket connect* (as, in fact, disclosed by Patel et al. in Fig. 5, socket 512) or as a *through hole connect* in a through hole structure, **neither** a socket **nor** a through hole structure being positively claimed by the Applicant and therefore **neither** socket **nor** through hole structure required to be met by the prior art. The Applicant's recitation "through hole connect" is merely a recitation of the **intended use** of a pin: It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987).

Or, in the alternative, Rejection #2 of Claim 1:

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 9, 10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al. in view of Li.

As to Claim 1:

I. Patel et al. discloses, in Fig. 5, an adapter (interposer) 506 comprising: a first (top) and a second (bottom) surface; first interconnects, i.e., the pads, not shown, on the first surface of adapter 506 that receive and electrically connect the BGA bumps of carrier 502 to adapter 506; second interconnects (pins 508; col.4: 62-66) on the second surface; since second interconnects 508 supply power to step down converter (SDC) 518 on carrier 502 (col.4: 66), then at least one connective path inherently exists between the first and second interconnects; a signal modifying circuit (comprising input capacitor 522 and input inductor 524) between the first interconnects and second interconnects 508, as disclosed in an alternate case of the Fig. 5 embodiment wherein said input capacitor 522 and input inductor 524 are mounted on the adapter 506, as in the embodiment of Fig. 3 (Fig. 3 and col.3: 63-64; Fig. 5 and col.5: 14-15).

II. Patel et al. discloses that second interconnects 508 are pins which function as *socket connects* for insertion into socket 512 (col.4: 62-66). Patel et al. does not teach that second interconnects 508 are "through hole connects;" i.e., pins intended for use as pin connectors for direct insertion into the through holes of a printed circuit board or the through holes of some other circuit substrate.

III. Li discloses a package 400 comprising a die 430 mounted on an adapter (interposer) 412, said adapter having first (pad) interconnects on the top surface thereof that receive the solder balls 422, and second (pin) interconnects on the bottom surface thereof that function equivalently as socket connects in one embodiment (for insertion into a socket, not shown, that is surface mounted on a printed circuit board 440) and as

through hole connects in another embodiment (for insertion directly into through holes of the printed circuit board as shown in Fig. 4) (col.4: 47-54).

IV. Since Patel et al. and Li are both in the electronic packaging art requiring board adapters for mounting electronic devices onto a printed circuit board, and since Li discloses that the second (pin) interconnects can be inserted into a socket on a printed circuit board, or, alternatively, directly into the through holes of a printed circuit board, then the art-recognized, applications dependent equivalent of mounting the second (pin) interconnects directly into the through holes of a printed circuit board for packaging applications not requiring or unable to support a socket would have been readily recognized as a practical package modification in the pertinent art of Patel et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the package of Patel et al. by removing the socket 512 (and socket 514 as well) and directly connecting second (pin) interconnects 508 into the through holes of printed circuit board (PCB) 516 for applications that do not require or cannot support a socket; e.g., applications requiring a smaller, lighter, less expensive package and/or requiring a direct adapter-to-PCB connection which provides a reduction in signal noise (sockets are noisy connections because their contacts contribute to parasitic inductance at higher signal frequencies).

As to Claim 2, Patel et al. further discloses that said first interconnects are physically spaced to correspond to a first pin configuration (i.e., BGA or PGA of carrier 502) of a power module, the power module comprising BGA carrier 502 and SDC 518

(Fig. 5; col.5: 6-8). Note that the BGA (ball grid array) of carrier (package) 502 is disclosed as a PGA (pin grid array) in an alternate embodiment (col.3: 40-42).

As to Claim 3, Patel et al. further discloses that the second interconnects 508 are physically spaced to correspond to a second pin configuration of an end user's circuit board 516 by way of the circuit board socket 512 (Fig. 5; col.4: 64-66) or by direct connection to the through holes of circuit board 516 in Patel et al. as modified, above, by Li (see Li, Fig. 4 and col.4: 46-54).

As to Claim 4, Patel et al. further discloses that a signal modifying circuit (i.e., input capacitor 522 and input inductor 524 mounted on adapter 506 in the alternative embodiment of Fig. 5, as indicated in col.5: 14-15) acts upon an input to the adapter 506 (just as in the embodiment of Fig. 3; col.3: 63-64).

As to Claim 5, Patel et al. further discloses that a signal modifying circuit (i.e., output capacitor 526 and output inductor 528 mounted on adapter 506; col.5: 11-12) acts upon an output to the adapter 506 (just as in the embodiment of Fig. 3; col.3: 64-65).

As to Claim 6, Patel et al. further discloses that the power module is a DC-to-DC converter (the DC power originates with a battery and a voltage regulator circuit provides a steady DC voltage having the correct amplitude; col.1: 11-16).

As to Claim 7, Patel et al. further discloses that the power module is an AC-to-DC converter (the DC power has been converted from AC power and a voltage regulator circuit provides a steady DC voltage having the correct amplitude; col.1: 11-16 and 29-32).

As to Claim 9, Patel et al. further discloses that, in the case where the first interconnects receive BGA bumps of the carrier 502 (col.3: 40-42), said first interconnects inherently comprise surface mount connects.

As to Claim 10, Patel et al. further discloses that, in the case where the first interconnects receive PGA pins of the carrier 502 (col.3: 40-42), said first interconnects inherently comprise through-hole connects.

As to Claim 13, Patel et al. further discloses that the signal modifying circuit--input capacitor 522 and input inductor 524 (col.5: 14-15)--comprises a filter; i.e., the signal modifying circuit filters the input power (just as in the Fig. 3 embodiment; col.3: 63-64).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al. (or, in the alternative, Patel et al. in view of Li) and further in view of Iversen et al.

I. Patel et al. discloses all the limitations of the claim including the power module comprising carrier 502 and converter 518 (col.5: 4-6), the power module disclosed as capable of DC-to-DC conversion or AC-to-DC conversion (col.1: 11-16). Patel et al.

further discloses that the power module disclosed provides reduced parasitic inductance and resistance in high frequency and high current applications (col.2: 49-60).

II. Patel et al. does not teach a DC-to-AC inverter.

III. Iversen et al. discloses a power delivery system that, among other things, provides reduced parasitic inductance and resistance in high frequency and high current applications (col.1: 47-56; col.4: 3-6), wherein the power delivery system may be any one of AC-to-AC and DC-to-DC converters, AC-to-DC rectifiers and DC-to-AC inverters (col.3: 47-54), depending on the requirements of the application.

IV. Since both Patel et al. and Iversen et al. both teach power delivery systems to a variety of high frequency and high current electrical and electronic applications, then the use of a DC-to-AC inverter power delivery system, taught by Iversen et al., for an application requiring AC power from a DC source would have been readily recognized in the power delivery system of the pertinent art of Patel et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the power module of Patel et al. so that it delivers power as a DC-to-AC inverter for applications requiring AC power from a DC source, as taught by Iversen et al.

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al. (or, in the alternative, Patel et al. in view of Li) and further in view of McDonnal.

I. Patel et al. discloses all the limitations of the claim and further teaches a power module package, i.e., a DC-to-DC converter comprising the carrier 502 and the SDC 518 mounted thereon (Fig. 5; col.1: 11-13 and 21-24; col.3: 31-35).

II. Patel et al. does not teach that the signal modifying circuit--input capacitor 522 and input inductor 524 (col.3: 63-64 and col.5: 14-15)--comprises an overvoltage protection device.

III. McDonnal discloses a DC-to-DC converter (Fig. 1) comprising an overvoltage protection device (circuit 80; col.4: 20-23) for the purpose of protecting the electrical system and the converter that provides the system power.

IV. Since McDonnal and Patel et al. both teach DC-to-DC converters for providing DC power to an electrical system, then an overvoltage circuit incorporated into the DC-to-DC converter, as taught by McDonnal, would have been readily recognized in the pertinent art of Patel et al. as a vital feature ensuring the reliability and safety of the DC-to-DC converter and electronic system to which the converter supplies the DC power.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate an overvoltage circuit in the power module package (i.e., the DC-to-DC converter) of Patel et al., as taught by McDonnal, in order to ensure the reliability and safety of the electronic system on adapter 506 and user circuit board 516 of Patel et al.

Response to Arguments

8. Applicant's arguments with respect to Claims 1-10, 13 and 14 have been considered but are moot in view of the new ground(s) of rejection. The Examiner has reconsidered and withdrawn the indication allowability of "the second interconnects

comprise through hole connects" from cancelled Claim 12. Both 35 USC § 102(e) and 35 USC § 103(a) rejections have been made of amended Claim 1 which incorporates said indicated subject matter in the recitation "the at least one second interconnect comprising a through hole contact." The 35 USC § 102(e) rejection of Claim 1 is due to the Examiner's reconsideration of the language of the claim with respect to what is and what is not positively claimed structure. The 35 USC § 103(a) rejection of Claim 1 gives weight, *for the sake of argument only*, to the Applicant's **intended use** claim language in order to apply newly discovered prior art (US Patent 6,525,944 B1 to Li) which clearly teaches that the adapter (interposer) pins may be used either as *socket connects* (for connection to a printed circuit board by way of a board-mounted socket) or, alternatively, as *through hole connects* (for direct connection to the through holes of a printed circuit board).

9. Since the Examiner has withdrawn the indication of allowability for the subject matter of cancelled Claim 12 (incorporated into amended Claim 1) and raised new grounds of rejection of amended Claim 1, the present Office Action is made NON-FINAL.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Examiner
Art Unit 2827

jbv
March 4, 2003